REMARKS

Claims 1 through 42 are currently pending in the application.

This reply is in response to the final Office Action of August 28, 2002.

Claims 1 through 42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Aoki et al. (United States Patent 5,629,539) in view of Iacoponi (United States Patent 5,545,592).

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Turning to the cited prior art, Aoki et al. describes memory cells of a DRAM comprising a pair of a MOS transistor and a capacitor located in a memory cell forming area on a semiconductor substrate in a matrix manner (rows and columns directions). (Col. 6 lines 66 – col. 7, line 2). Each memory cell is connected to one of a plurality of bit lines arranged in parallel in a column direction and is connected to one of a plurality of word lines arranged in parallel in a row direction. (See Fig. 1A and col.7, lines 2-6). Aoki et al. also describes a gate electrode 13, formed of polycrystalline silicon with a gate insulating film 12 in between, formed on an element area 8 surrounded by an element separation area 11 of a p-type Si substrate 10. (See Fig. 1B, and col. 7, lines13-16). Silicon nitride films 14 and 16 are formed on the upper and side portions of the gate electrode 13. N-type diffusion layers 15a and 15b serve as source and drain regions and are formed on the substrate surface adjacent to gate electrode 13. (Col. 7, lines 16-20). Gate electrode 13 is used as a word line. A structure 13a, similar to gate electrode 13, is formed on the element separation area 11 and is a passing word line for memory cells adjacent to each other. (Col. 7, lines 20-25).

A cylindrical storage node electrode 21b serves as one electrode of the capacitor, and is formed on the n-type diffusion layer 15b. This n-type diffusion layer is to be mounted on the

adjacent gate electrode 13 and the passing word line 13a. In addition, a pad electrode 21a for a bit line contact, having the same structure as the storage node electrode 21b is formed on the n-type diffusion layer 15b. Conductive material 24a is embedded in the pad electrode 21a to form a plug electrode. Conductive material 24a is projected to an upper position relative to the end of the pad electrode 21a. After this step a capacitor dielectric film 27 is formed on the surface of the pug electrode (comprising 21a and 24a). Only the upper surface of the conductive material 24a is not covered, and it is here that plate electrode 28 is formed. An interlayer insulating film 31 is formed to flatten the embedding surface of each portion and a bit line 33 is formed on the interlayer insulating film 31 to be connected to the conductive material 24a. (Col. 7, lines 25-43).

Iacoponi is directed to a nitrogen treatment for metal-silicide contact. A low-resistance electrical contact to a silicon body is created by first forming a titanium silicide layer on the underlying silicon by depositing titanium metal on the silicon body and then subjecting the silicon body to a high-temperature annealing process. (Col. 2, lines 36-41). A layer of dielectric, such as silicon dioxide is then deposited on the titanium silicide layer. Contact holes are then etched through the dielectric layer in order to uncover a portion of the underlying titanium silicide layer. (Col. 2, lines 41-44). This uncovered titanium silicide layer is then exposed to a plasma of active free nitrogen, which acts to convert some of the exposed titanium silicide surface to titanium nitride. A second layer of titanium nitride is then deposited over the converted titanium nitride. The contact is completed by depositing a layer of tungsten over the second layer of titanium nitride to contact the exposed titanium nitride over the titanium silicide layer. (Col. 2, lines 44-53).

Applicants respectfully submit that the rejections of claims 1 through 42 under 35 U.S.C. § 103(a) fail to establish a *prima facie* case of obviousness.

First, there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Aoki et al. with the teachings of Iacoponi as has been presented by the Examiner. Aoki et al. involves a stacked capacitor construction that involves multiple depositions to achieve the plug contacts. (Col. 8, lines 2-5, col. 8 lines 5-8, col. 8 lines 17-21, col. 8 lines 26-34). Iacoponi on the other hand is specifically directed to a simpler method designed to overcome defect formation caused by the

reaction of tungsten hexafluoride with the titanium layer. (Col. 2, lines 8-13). Neither Aoki et al. not Iacoponi is directed toward a method of forming an electrical connection in a high aspect ratio contact hole. Additionally, Aoki et al. overcomes density problems by widening the space for a capacitor contact opening and therefore does not suffer from the aspect ration issues addressed by Applicant's invention. Aoki et al. overcomes the reaction problem of Iacoponi by multiple depositions which ensure that no contact occurs between the tungsten hexafluoride gas and the titanium layer and thus need not address the reaction problem. Furthermore, Iacoponi is aimed at reducing processing steps.

Secondly, Applicants suggest that it would not be obvious to combine the method of Aoki et al., which involves multiple depositions and repeated etch-back of material, with Iacoponi. Iacoponi is specifically directed toward a simple yet reliable nitrogen treatment designed to reduce defect formation caused by the reaction of tungsten hexafluoride gas with exposed elemental titanium. Iacoponi teaches away from adding process steps and thus is incompatible with the complex processes of Aoki et al. Neither Aoki et al. nor Iacoponi teaches or suggests any techniques to minimize the problems associated with high aspect ratio contact plugs. Applicant respectfully suggests that the combination is the result of impermissible hindsight afforded by Applicant's invention and not as a result of any express or inherent suggestion in the claimed references.

In view of the foregoing, Applicants respectfully submit the combination of Aoki et al. and Iacoponi fail to establish a prima facie case of obviousness under the provisions of 35 U.S.C. § 103(a) and that claims 1 through 42 are clearly allowable over the cited prior art.

Applicants request the entry of this amendment for the following reasons:

The amendment clearly points out why the cited prior art fails to establish a *prima* facie case of obviousness under 35 U.S.C. § 103 regarding the claimed invention thereby placing the application in condition for allowance.

The amendment is timely filed.

The amendment does not require any further search or consideration as no claim has been amended.

In summary, Applicants request entry of this amendment, the allowance of claims 1 through 42, and the case passed for issue.

Respectfully submitted,

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